We claim:

1. A method for fabricating a stacked gate array on a semiconductor wafer with a diameter of more than 8 inch comprising the steps of:
- Providing a reaction chamber having an upper inductive means and a lower capacitive means;
- Adjusting power settings of said upper inductive means for obtaining a uniformity better than 10% in etching a wafer with a diameter of 8 inch at a rate of etching between 50 and 500 nm/min;
- Placing said wafer with a diameter of more 8 inch into said reaction chamber; and
- Plasma etching said wafer with a diameter of more than 8 inch to provide said stacked gate array.

2. The method according to claim 1, wherein said stacked gate array comprises a layer of polysilicon on a layer of oxide.

3. The method according to claim 1, wherein said stacked gate array comprises a layer of polysilicon, a layer of tungsten-silicon and a layer of oxide.

4. The method according to claim 1, wherein said stacked gate array comprises a layer of polysilicon, a layer of titanium-silicon and a layer of oxide.

5. The method according to claim 1, wherein said step of plasma etching comprises the steps of:
- Feeding at least one etching gas into said reaction chamber;
- Energising said inductive and capacitive means to convert the etching gas into a plasma to etch said wafer.

6. The method according to claim 5, wherein the gas flow, the pressure and the temperature of said etching gas is such that said adsorption rate is bigger than a desorption rate of gas particles on a surface of said wafer.

7. The method according to claim 5, wherein further the method comprises the step of recreating said reaction chamber before said step of plasma etching.

8. The method according to claim 5, wherein said etching gas comprises at least one gas of the group HCl, Cl_2, NF_3, O_2 and HBr.

9. The method according to claim 1, wherein said power of said upper inductive means is adjusted to between 50 and 600 Watts.

10. The method according to claim 1, wherein said power of said lower capacitive means is adjusted to between about 0 and 200 Watts.

11. The method according to claim 1, further comprising the step of adjusting said lower capacitive means to a power setting of less than 300 Watts.

12. The method according to claim 11, wherein said power of said upper inductive means is adjusted to between 50 and 600 Watts and said power of said lower capacitive means is adjusted to between 0 and 200 Watts.

13. The method according to claim 1, wherein the power of said upper inductive means is adjusted to obtain a uniformity of better than 5% in etching a wafer with a diameter of 8 inch at a rate of etching between 200 and 400 nm/min.

14. A method for etching a semiconductor wafer with a diameter of 10 or more inch comprising the steps of:

- Providing a reaction chamber having an upper inductive means and a lower capacitive means;
- Adjusting power settings of said upper inductive means which are suited to etch a wafer with a diameter of 8 inch to obatin stacked gates of MOSFETs on said wafer of 8 inch;
- Placing said wafer with a diameter of 10 or more inch into said reaction chamber; and
- Plasma etching said wafer with a diameter of 10 or more inch to obtain stacked gates of MOSFETs.

15. The method according to claim 14, wherein said wafer to be etched comprises a layer of a metal silicide over a layer of polysilicon over a layer of a gate oxide.

16. The method according to claim 15, wherein the plasma etching of the wafer having a diameter of 10 or more inch is performed using an etch gas composition comprising HCl, Cl_2 and NF_3 for etching the metal silicide, using an etch gas composition comprising HCL, Cl_2 and O_2 for etching the polysilicon and using an etch gas composition comprising HBr and at least one of Cl_2 and O_2 when approching the gate oxide layer.

17. A method for etching a semiconductor wafer with a diameter of 10 or more inch comprising the steps of:

- Providing a reaction chamber having an upper inductive means and a lower capacitive means;
- Adjusting power settings of said upper inductive means to between 50 and 600 Watts;
- Adjusting power settings of said lower capacitive means to less than 200 Watts;

- Providing a wafer having a layer of a metal silicide, a layer of polysilicon and a layer of a gate oxide;
- Placing said wafer into said reaction chamber; and
- Plasma etching said wafer relative to a mask thereby removing said layers of metal silicide and polysilicon where not protected by said mask and maintaining said layers of metal silicide and polysilicon and gate oxide where protected by said mask in order to obtain stacked transistor gates.

18. The method according to claim 16, wherein the plasma etching of the wafer having a diameter of 10 or more inch is performed using an etch gas composition comprising HCl, Cl_2 and NF_3 for etching the silicide, using an etch gas composition comprising HCL, Cl_2 and O_2 for etching the polysilicon and using an etch gas composition comprising HBr and at least one of Cl_2 and O_2 when approching the gate oxide layer.